# An Electrothermal BSIM3 Model for Large-Signal Operation of RF Power LDMOS Devices

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*Abstract* — **An electrothermal BSIM3 model for large-signal operation of RF power LDMOS devices has been developed. The physically-based model was carefully calibrated to pulsed current/voltage characteristics and bias-dependent capacitance measurements. Internal matching networks and influence from the package were included in a physical way. The implemented electrothermal coupling exhibited good numerical stability during large-signal operation and the model correlates well to measurements of RF functional characteristics.**

## I. INTRODUCTION

Power amplifier design in base stations for wireless communication becomes more and more challenging. The introduction of the third-generation (3G) systems set even higher requirements on linearity, and tighter tolerances on RF characteristics on LDMOS devices used in the design. Accurate models become more and more important in the design work. The RF power devices used in wireless systems are particularly challenging to model since they operate at both high powers and high frequencies. These large devices have very low impedances, which present difficulties when working with standard 50-ohm test equipment. They operate in class AB under large-signal conditions, and the high powers also make it necessary to take self-heating into account.

In the past, most compact models for RF applications have been of an empirical nature (e.g. [1-3]). Several physically-based models have also been proposed (e.g. [4],[5]). In this work, a physically-based model based on BSIM3 and extended with electrothermal coupling is presented. To our knowledge, this is the first BSIM3 model including self-heating; it is targeted towards RF power LDMOS devices and power amplifier design in wireless systems. A physically-based model such as the BSIM3 (even though relatively complex) can be an advantage for accurate calibration to measurements. It also serves as a helpful tool in die development, both for sensitivity analysis of process variations in the wafer fab and for prediction of performance induced by design changes. The presented model includes die, internal matching networks and package and will be discussed in that order. The implementation of the electrothermal coupling will be described in a separate section. Finally, correlation between measured and simulated RF characteristics is shown.

## II. DIE MODEL

### A. *Pulsed IV-measurements*

An important point in the calibration of an electrothermal model is to decouple electrical and thermal characteristics. A pulsed measurement system for current/voltage characteristics was therefore developed; it was designed for characterization of full-sized devices. It employs a signal generator, oscilloscope and a DC power supply. The system is controlled from a PC and the collection of data is automated. The data is collected after (typically) ~ 3 µs with a (typical) duty-cycle of 0.01 %. (Compared to a commercial curve tracer such as a Tektronix 371A with a pulse width of 250 µs and a duty-cycle of ~ 0.3 %, this makes a large difference for the high current operating region.) The full-sized packaged devices were attached to a thermal chuck of a SIGMA temperature-controlled system (T= -100°C to T=200°C). Thus, pulsed measurements can be taken over a wide range of accurately controlled isothermal temperatures. Figure 1 shows measured pulsed data (symbols) taken at temperatures T=25°C, T=75°C and T=125°C. Solid lines denote the model, which will be discussed next.

### B. *Intrinsic device model*

Figure 2 shows a schematic of the die model. It consists of a BSIM3 model, surrounded by a non-linear resistor, a voltage-dependent capacitance $C_{dg}$, a constant capacitance $C_{gs}$, a SPICE diode containing a voltage-dependent $C_{ds}$ and gate and source resistances $R_g$ and $R_s$. Power sensing elements at the input and output of the power LDMOS feed dissipated power into a thermal circuit and the temperature rise is coupled back to the BSIM3 model and the non-linear resistor (see next section).

The calibration of the model starts at low currents (here the influence of the nonlinear resistor is negligible). Physical parameters such as gate length, oxide thickness



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and junction depths were locked from process simulation or direct measurements. The BSIM3 parameters were extracted from $I_d$ - $V_{gs}$ and $I_d$ - $V_{ds}$ characteristics. It should be stated that several of the parameters taking higher order effects into account were neglected at this point by either setting them to very small or very large values. However, the large number of parameters available in the BSIM3 gives opportunities to improve the accuracy of the model further on, if needed, and extend it to a wider range of operating conditions, possibly take failure modes into account, etc. Parameters for temperature dependence, mainly threshold voltage and mobility, were extracted for good correlation over the temperature range T=25°C to T=125°C.

Power LDMOS devices are subject to quasi-saturation for high gate voltages [6,7]; the reason is current saturation in the LDD region at high current levels. The non-linear resistance of the LDD region has two voltage-dependencies [7], one for gate-source voltage ($V_{gs}$) and another one for drain-source voltage ($V_{ds}$). For high gate voltages, the difference in drain current due to quasi-saturation in a power LDMOS is very large. This behavior is not included in the BSIM3 and it is desirable to create a physically-based model for the LDD region. Currently, the non-linear resistor was extracted in the following way: the BSIM3 parameters were locked for good correlation in the low current region, a resistance was extracted in an automated matlab-script for the high current region by subtracting the drain-source voltage of the measurement from the simulation at each point. A function containing exponential and power-law dependencies fit the resulting non-linear resistor with gate-source and drain-source voltage dependencies. This was repeated for temperatures in the range T=25°C to T=125°C and temperature-dependent parameters were introduced. Figure 1 shows the end-result of the BSIM3 extraction including the non-linear resistor for gate voltages $V_{gs}$=4 to $V_{gs}$=10 V (steps 0.5 V) at the temperatures T=25°C, T=75°C and T=125°C. The correlation shown is acceptable.

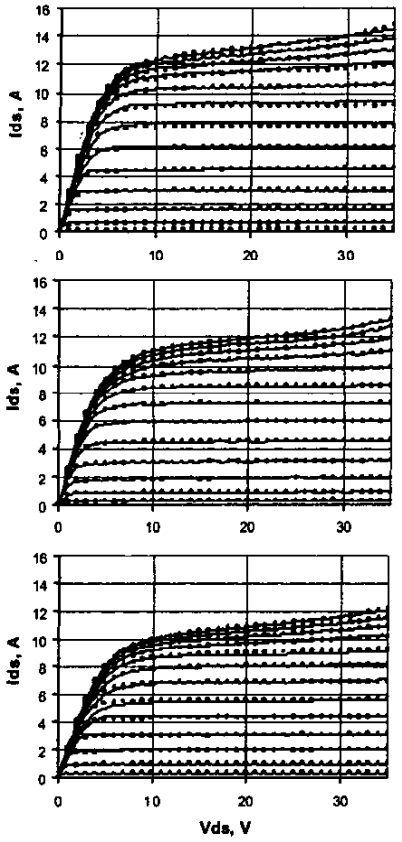


**FIGURE 1** Current/voltage characteristics. Symbols represent pulsed IV-data and solid lines represent the model. a) T=25°C b) T=75°C and c) T=125°C. Vgs: 4 – 10 V with step 0.5 V.

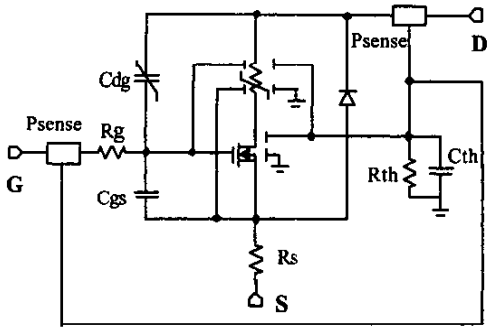


**FIGURE. 2** Schematic of die model: BSIM3 and non-linear resistor with electro-thermal coupling, external $C_{dg}$ and $C_{gs}$, gate and source resistors, diode, power sensing elements and thermal circuit.

Power LDMOS devices show a different behavior for the bias-dependence of capacitances compared to conventional MOSFETs [1]. The capacitances are therefore modeled with external elements. The bias-dependent capacitances were determined from CV-measurements on full-scale devices. Figure 3 shows measured (symbols) and fitted functions (solid lines) for $C_{dg}$ and $C_{ds}$. In the current model, $C_{dg}$ is modeled with a $V_{dg}$ voltage-dependence. $C_{ds}$ and associated $V_{ds}$-dependence is modeled through a SPICE diode; this also takes the possibilities of over-drive into account (forward-biasing of the diode). $C_{gs}$ was found to be independent of drain-source voltage for the full-sized device and was therefore modeled with a constant capacitor. Conventionally, bias-dependent capacitances are extracted from small-signal models and s-parameter measurements. In the case of high

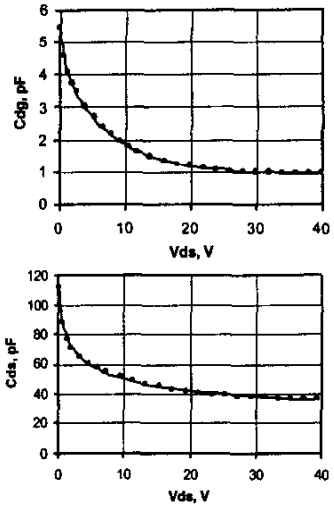


**FIGURE 3.** Voltage dependencies of capacitances on full-scale devices. a) $C_{dg}$ b) $C_{ds}$.

power LDMOS devices with very low impedances, s-parameter measurements on full-scale devices with varied bias is extremely challenging. These challenges stem from potential damage to test equipment as well as difficulties in calibration and definition of reference planes, which can lead to large measurement errors. Modeling of full-scale devices based on s-parameter measurements on small test-structures relies on accurate scaling rules and needs further study.

### *C. Implementation of electro-thermal coupling*

As shown in Figure 2, an extra node has been added to the BSIM3 model for the temperature dependence; a similar node was added to the non-linear resistor. Dissipated power is calculated by power sensing elements on the input and output of the device. The powers are added together and fed into a thermal circuit where the voltage over the thermal network represents the temperature increase, which is fed back to the BSIM3 and the non-linear resistor. All temperature dependencies in the BSIM3 were accounted for by substitution of the temperature as a parameter to a variable provided by the extra node; the temperature dependence for the non-linear resistor was implemented in the same way. The model has been implemented in Microwave Office (provided by Applied Wave Research) by making changes directly in the BSIM3 source code. The thermal network can be extended by the user to account for effects of heat flanges, influence of the PC board etc.

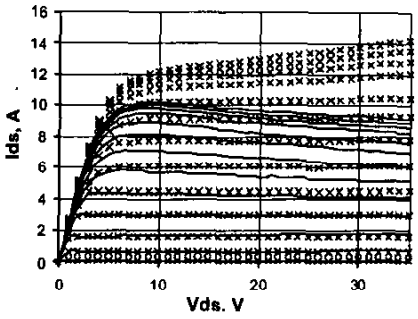


**FIGURE 4** Current/voltage characteristics including electro-thermal coupling. $R_{th}$=0 K/W (symbols) and $R_{th}$=0.85 K/W (solid line). $V_{gs}$= 4 - 10 V in steps of 0.5 V.

Figure 4 shows the dependence of current/voltage characteristics on thermal resistance. Symbols denote a simulation with Rth=0 K/W (corresponding to no influence of heating) and solid lines denote $R_{th}$=0.85 K/W. There is a substantial difference for higher gate voltages. The value 0.85 K/W was extracted from thermal resistance measurements using an IR camera; this value was used in the RF simulations performed in this study (section IV).

## III. MATCHING NETWORKS AND PACKAGE

Figure 5 shows a schematic of the full model, including internal matching networks and influence from the package. Input and output matching networks, consisting of bonding wires and off-chip capacitors are modeled with lumped elements. Inductances were extracted from direct measurements of bond loop heights and shapes and subsequent analytical calculations including mutual coupling between wires; cross-coupling between drain and gate bonding wires was ignored due to the large distance between them in this design. The influence of the package is modeled with two transmission lines. These elements represent the physical parts of the gate and drain contact

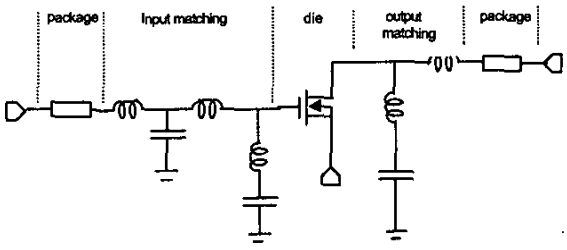


**FIGURE 5.** Schematic of full model including internal matching networks and influence from the package.

leads from the end of the package to the actual contact on the circuit board.

## IV. VALIDATION OF RF-CHARACTERISTICS

In the validation of functional RF characteristics of the model, the test circuit was included in the simulation (excluded here due to lack of space); the circuit elements in the test circuit were modeled with ideal lumped elements and ideal transmission lines. Figure 6 shows gain, output power and efficiency as a function of input power. The measured and simulated data are seen to correlate very well. Additionally, the model gives a reasonable agreement for third order intermodulation distortion as shown in Figure 7; the model predicts a "sweet-spot" that qualitatively agrees well with measurements. The quantitative discrepancy is largest for low output powers where IM3 is very sensitive to small changes in drain quiescent current (Idq) setting induced by variations between test circuits, fluctuations in temperature, etc.; this will be analyzed further.

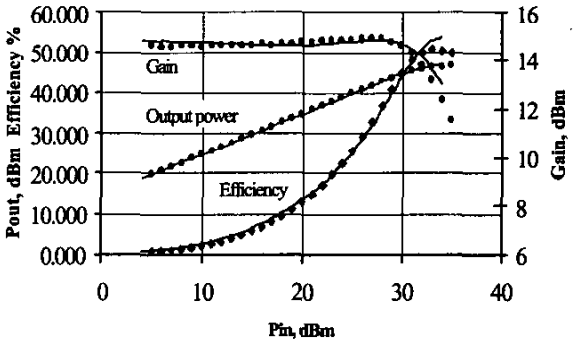


**FIGURE 6** Gain, output power and efficiency versus input power.

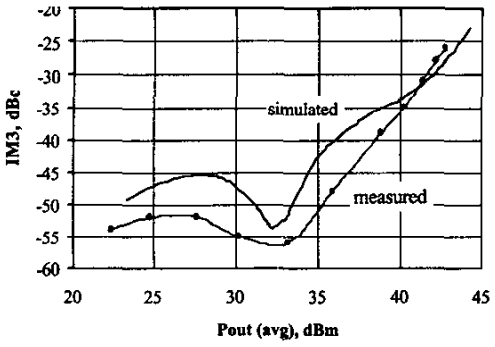


**FIGURE 7** Third order intermodulation distortion as a function of average output power.

## V. CONCLUSIONS

An electrothermal BSIM3 model for large-signal operation of RF power LDMOS devices has been developed. The physically-based model was carefully calibrated to pulsed current/voltage characteristics and bias-dependent capacitance measurements. Internal matching networks and influence from the package was included in a physical way. The implemented electrothermal coupling was seen to exhibit numerical stability during large-signal operation. Measured and simulated basic RF characteristics correlate very well and the model gives reasonable agreement for third order intermodulation distortion.

## ACKNOWLEDGEMENTS

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